Simulation Group Project

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Cache Implementation Summary

The cache struct contains a valid variable to mark if the slot is empty or not, a time variable to denote when the data was last accessed and used, and a tag variable to denote which slot in the cache is being accessed/used to store memory.

In the initialization of the simulation, a for loop runs through the sets and initializes the cache line struct with respect to the index and cache associativity by using calloc. There is also a nested for loop that initializes each individual cache slot per set with a 0 in the valid, time, and tag arrays.

Trap address calculated the tag using the address, block offset, and the associativity and proceeded to call the LRU functions based on whether or not the cache hit or missed.

For the LRU, we first checked each slot’s valid bit in the cache index to see if it was empty or not. On a miss, if there was an empty slot, we inserted the address with a valid bit of 1, a time equal to the access count, and the tag formed in trap address. On a miss with a full cache slot, we replaced the entry with the lowest time count using the same information as above. On a hit, we only change the time variable.

Pipeline Implementation Summary

For the pipeline functions, each instruction pushed the pipeline stage when called. Each function also defined the itype with a keyword and uses the input information to store data about each instruction. In the push stage function, once it passes the instruction check, it checks for the BRANCH itype and then adds to the branch count, checks whether the branch is taken or not, compares that to the predictor and then either adds one cycle on missed prediction, or increments the correct predictions. After BRANCH it checks the LW itype, where it calls trap address and adds cycles on a miss. Following LW, it checks SW, where it also calls trap address and adds cycles. Then it adds one cycle for natural progression, and proceeds to push the pipeline through its stages. After the pipeline is pushed through, it is set to NOP and ends.

Performance Evaluation All Configurations

1 Word, Direct Mapped

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 0

Cache Configuration

Index: 7 bits or 128 lines

BlockSize: 1

Associativity: 1

BlockOffSetBits: 2

CacheSize: 7168

Cache Performance

Number of Cache Accesses is 35676

Number of Cache Misses is 1113

Number of Cache Hits is 34563

Cache Miss Rate is 0.031197

Pipeline Performance

Total Cycles is 45419

Total Instructions is 34129

Total Branch Instructions is 7020

Total Correct Branch Predictions is 5730

CPI is 1.330804

1 Word, 2-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 0

Cache Configuration

Index: 6 bits or 64 lines

BlockSize: 1

Associativity: 2

BlockOffSetBits: 2

CacheSize: 7296

Cache Performance

Number of Cache Accesses is 35780

Number of Cache Misses is 480

Number of Cache Hits is 35300

Cache Miss Rate is 0.013415

Pipeline Performance

Total Cycles is 40049

Total Instructions is 34449

Total Branch Instructions is 7031

Total Correct Branch Predictions is 5734

CPI is 1.162559

1 Word, 4-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 0

Cache Configuration

Index: 5 bits or 32 lines

BlockSize: 1

Associativity: 4

BlockOffSetBits: 2

CacheSize: 7424

Cache Performance

Number of Cache Accesses is 35823

Number of Cache Misses is 349

Number of Cache Hits is 35474

Cache Miss Rate is 0.009742

Pipeline Performance

Total Cycles is 38975

Total Instructions is 34550

Total Branch Instructions is 7036

Total Correct Branch Predictions is 5744

CPI is 1.128075

2 Word, Direct Mapped

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 0

Cache Configuration

Index: 6 bits or 64 lines

BlockSize: 2

Associativity: 1

BlockOffSetBits: 3

CacheSize: 5632

Cache Performance

Number of Cache Accesses is 35691

Number of Cache Misses is 1027

Number of Cache Hits is 34664

Cache Miss Rate is 0.028775

Pipeline Performance

Total Cycles is 44738

Total Instructions is 34212

Total Branch Instructions is 7015

Total Correct Branch Predictions is 5714

CPI is 1.307670

2 Word, 2-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 0

Cache Configuration

Index: 5 bits or 32 lines

BlockSize: 2

Associativity: 2

BlockOffSetBits: 3

CacheSize: 5696

Cache Performance

Number of Cache Accesses is 35793

Number of Cache Misses is 349

Number of Cache Hits is 35444

Cache Miss Rate is 0.009751

Pipeline Performance

Total Cycles is 38982

Total Instructions is 34551

Total Branch Instructions is 7042

Total Correct Branch Predictions is 5734

CPI is 1.128245

2 Word, 4-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 0

Cache Configuration

Index: 4 bits or 16 lines

BlockSize: 2

Associativity: 4

BlockOffSetBits: 3

CacheSize: 5760

Cache Performance

Number of Cache Accesses is 35841

Number of Cache Misses is 197

Number of Cache Hits is 35644

Cache Miss Rate is 0.005496

Pipeline Performance

Total Cycles is 37710

Total Instructions is 34647

Total Branch Instructions is 7042

Total Correct Branch Predictions is 5744

CPI is 1.088406

4 Word, Direct Mapped

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 0

Cache Configuration

Index: 6 bits or 64 lines

BlockSize: 4

Associativity: 1

BlockOffSetBits: 4

CacheSize: 9664

Cache Performance

Number of Cache Accesses is 35835

Number of Cache Misses is 750

Number of Cache Hits is 35085

Cache Miss Rate is 0.020929

Pipeline Performance

Total Cycles is 42396

Total Instructions is 34362

Total Branch Instructions is 6997

Total Correct Branch Predictions is 5689

CPI is 1.233805

4 Word, 2-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 0

Cache Configuration

Index: 5 bits or 32 lines

BlockSize: 4

Associativity: 2

BlockOffSetBits: 4

CacheSize: 9728

Cache Performance

Number of Cache Accesses is 35855

Number of Cache Misses is 144

Number of Cache Hits is 35711

Cache Miss Rate is 0.004016

Pipeline Performance

Total Cycles is 37268

Total Instructions is 34681

Total Branch Instructions is 7043

Total Correct Branch Predictions is 5748

CPI is 1.074594

4 Word, 4-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 0

Cache Configuration

Index: 4 bits or 16 lines

BlockSize: 4

Associativity: 4

BlockOffSetBits: 4

CacheSize: 9792

Cache Performance

Number of Cache Accesses is 35855

Number of Cache Misses is 78

Number of Cache Hits is 35777

Cache Miss Rate is 0.002175

Pipeline Performance

Total Cycles is 36694

Total Instructions is 34701

Total Branch Instructions is 7043

Total Correct Branch Predictions is 5748

CPI is 1.057434

1 Word, Direct Mapped

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 1

Cache Configuration

Index: 7 bits or 128 lines

BlockSize: 1

Associativity: 1

BlockOffSetBits: 2

CacheSize: 7168

Cache Performance

Number of Cache Accesses is 35676

Number of Cache Misses is 1113

Number of Cache Hits is 34563

Cache Miss Rate is 0.031197

Pipeline Performance

Total Cycles is 49876

Total Instructions is 34129

Total Branch Instructions is 7020

Total Correct Branch Predictions is 1273

CPI is 1.461396

1 Word, 2-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 1

Cache Configuration

Index: 6 bits or 64 lines

BlockSize: 1

Associativity: 2

BlockOffSetBits: 2

CacheSize: 7296

Cache Performance

Number of Cache Accesses is 35780

Number of Cache Misses is 480

Number of Cache Hits is 35300

Cache Miss Rate is 0.013415

Pipeline Performance

Total Cycles is 44503

Total Instructions is 34449

Total Branch Instructions is 7031

Total Correct Branch Predictions is 1280

CPI is 1.291852

1 Word, 4-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 1

Cache Configuration

Index: 5 bits or 32 lines

BlockSize: 1

Associativity: 4

BlockOffSetBits: 2

CacheSize: 7424

Cache Performance

Number of Cache Accesses is 35823

Number of Cache Misses is 349

Number of Cache Hits is 35474

Cache Miss Rate is 0.009742

Pipeline Performance

Total Cycles is 43435

Total Instructions is 34550

Total Branch Instructions is 7036

Total Correct Branch Predictions is 1284

CPI is 1.257164

2 Word, Direct Mapped

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 1

Cache Configuration

Index: 6 bits or 64 lines

BlockSize: 2

Associativity: 1

BlockOffSetBits: 3

CacheSize: 5632

Cache Performance

Number of Cache Accesses is 35691

Number of Cache Misses is 1027

Number of Cache Hits is 34664

Cache Miss Rate is 0.028775

Pipeline Performance

Total Cycles is 49169

Total Instructions is 34212

Total Branch Instructions is 7015

Total Correct Branch Predictions is 1283

CPI is 1.437186

2 Word, 2-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 1

Cache Configuration

Index: 5 bits or 32 lines

BlockSize: 2

Associativity: 2

BlockOffSetBits: 3

CacheSize: 5696

Cache Performance

Number of Cache Accesses is 35793

Number of Cache Misses is 349

Number of Cache Hits is 35444

Cache Miss Rate is 0.009751

Pipeline Performance

Total Cycles is 43426

Total Instructions is 34551

Total Branch Instructions is 7042

Total Correct Branch Predictions is 1290

CPI is 1.256867

2 Word, 4-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 1

Cache Configuration

Index: 4 bits or 16 lines

BlockSize: 2

Associativity: 4

BlockOffSetBits: 3

CacheSize: 5760

Cache Performance

Number of Cache Accesses is 35841

Number of Cache Misses is 197

Number of Cache Hits is 35644

Cache Miss Rate is 0.005496

Pipeline Performance

Total Cycles is 42164

Total Instructions is 34647

Total Branch Instructions is 7042

Total Correct Branch Predictions is 1290

CPI is 1.216960

4 Word, Direct Mapped

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 1

Cache Configuration

Index: 6 bits or 64 lines

BlockSize: 4

Associativity: 1

BlockOffSetBits: 4

CacheSize: 9664

Cache Performance

Number of Cache Accesses is 35835

Number of Cache Misses is 750

Number of Cache Hits is 35085

Cache Miss Rate is 0.020929

Pipeline Performance

Total Cycles is 46801

Total Instructions is 34362

Total Branch Instructions is 6997

Total Correct Branch Predictions is 1284

CPI is 1.361999

4 Word, 2-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 1

Cache Configuration

Index: 5 bits or 32 lines

BlockSize: 4

Associativity: 2

BlockOffSetBits: 4

CacheSize: 9728

Cache Performance

Number of Cache Accesses is 35855

Number of Cache Misses is 144

Number of Cache Hits is 35711

Cache Miss Rate is 0.004016

Pipeline Performance

Total Cycles is 41725

Total Instructions is 34681

Total Branch Instructions is 7043

Total Correct Branch Predictions is 1291

CPI is 1.203108

4 Word, 4-Way

Enter Branch Prediction: 0 (NOT taken), 1 (TAKEN): 1

Cache Configuration

Index: 4 bits or 16 lines

BlockSize: 4

Associativity: 4

BlockOffSetBits: 4

CacheSize: 9792

Cache Performance

Number of Cache Accesses is 35855

Number of Cache Misses is 78

Number of Cache Hits is 35777

Cache Miss Rate is 0.002175

Pipeline Performance

Total Cycles is 41151

Total Instructions is 34701

Total Branch Instructions is 7043

Total Correct Branch Predictions is 1291

CPI is 1.185874

**4 Word, 4-Way, predict Not taken was the most efficient**

Individual Tasks

The cache was mostly implemented by Billy, but we all spent a significant amount of time looking for bugs in the cache functions. The pipeline was mostly implemented by Subin/Alex. Testing efficiency and different cache builds was done by Subin/Billy, and the write-up was done by Alex.